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Wendy Beard

Profile

An enthusiastic and conscientious worker. Able to work under pressure in order to meet deadlines and project timescales. Extensive experience with a wide range of CAD tools, functional simulators, timing and power analysis tools. Well versed in all aspects of Physical Design from Floorplanning and Physical Synthesis to final Place & Route and Verification. Comprehensive background in full custom Mask Layout. Dedicated and adaptable with an enthusiasm for learning. Equally at ease working independently or as part of a team.

Experience

December 09 – January 2010 Sidense Corp., Ottawa, Canada

Physical Design Engineer (contract)

- Full custom analog circuit layout in Mentor ICStudio and ICstation
- Design verification using Calibre DRC & LVS tools.
- Technology design in EMM180 ALP33 process (0.18u)

April 08 - July 08, Oct 08 – Nov 08, April 09 – August 09 Kaben Wireless Silicon, Ottawa, Canada

Physical Design Engineer (contract)

- Full custom analog RF circuit layout in Cadence Virtuoso
- Design verification using both Assura and Calibre DRC & LVS tools.
- Technology design in TSMC 0.18u, IBM 7WL & IBM 8WL (BiCMOS)

March 2004 – April 2008 IDT Canada, Ottawa, Canada

Physical Design Engineer

- Responsible for floorplanning, CTS, place & route and timing closure, block integration, parasitic extraction, drc & lvs
- ASIC physical design using Synopsys Astro Suite and Magma Vortex
- Parasitic Extraction using Star-RCXT
- Design verification using Hercules DRC & LVS tools.
- Full custom layout in Cadence Virtuoso XL
- Technology design in 0.13u, 90nm and 65nm

Nov 2003 – Feb 2004 Siglobe Inc., Ottawa, Canada

Physical Design Engineer (Independent Contractor)

- ASIC physical design using Synopsys Astro Suite.
- Parasitic Extraction using Star-RCXT
- Design verification using Calibre DRC & LVS tools.

Sept 2003 – Nov 2003 Intronic Semiconductor, Gatineau, Canada

Physical Design Engineer (Independent Contractor)

- Full custom layout of Analog circuits using Cadence Virtuoso layout editor
- LEF generation
- Physical design and synthesis of mixed signal ASIC designs using Cadence SE and Ambit Build Gates Physical Compiler.
- Design verification using Dracula DRC & LVS tools.

July 2001 – April 2003 MOSAID Technologies Inc , Ottawa, Canada

Physical Design Engineer

- Physical design and synthesis of ASIC designs using Cadence SE and Synopsys Physical Compiler.
- Design verification using Calibre DRC & LVS tools.
- Static timing analysis with Synopsys PrimeTime and Cadence Pearl.
- Power analysis with Voltage Storm and Synplicity Power Planner.
- Crosstalk analysis and avoidance using CeltIC from Cadence Design Systems.
- Parasitic Extraction using Hyperextract and Fire & Ice.
- LEF generation with Cadence Abstract tool.
- Knowledge of Perl and Skill.
- Well versed in all aspects of current Cadence 5.4 SE-SI flow from floorplanning through placement and optimisation to final route with optimisation for timing and signal integrity.

Aug 1996–July 2001 Philips Semiconductors, Nijmegen, The Netherlands

Senior Library Engineer: Library Technology Group

- Responsible for Cadence back end standard cell core library views - layout, schematic, symbol and abstracts
- Developed and maintained Cadence DIVA DRC and LVS checksets for sign-off of basic views for use with Cadence SEDSM place & route tools.
- Expert in use of Sagantec Dream compaction tool, used successfully in the generation of three of the current core libraries.
- Team co-ordinator for two 0.35µ cell library migration projects, using manpower from Ireland, Bangalore and Nijmegen.
- Developed DfM actions with regard to the improvement of the libraries and generating test chips to verify functionality on silicon.
- Worked on production layout of 0.12µ digital core libraries and began implementing their migration to 0.10µ technology.

Nov 1994 – Aug 1996 Pijnenburg Microelectronics, Vught, NL

ASIC Physical Design Engineer

- Specialized in the use of back-end tools, with special responsibility for incorporating custom designed, hand laid-out analog and digital circuitry

into the ASIC designs

- Encompassed the full design cycle from characterizing blocks using Hspice to extract timing and functionality, to layout using Cadence's Virtuoso, Cell Ensemble and Cell3 and checking completed IC design using Cadence's Diva software.
- Liased with Cadence Technical Support and ES2/ATMEL foundry support teams with respect to design aspects and software issues.

July 1990– Sept 1994, Music Semiconductors, Eygelshoven, NL

IC Design Engineer

- Worked as part of a small team involved in full custom design of colour palette graphics chips.
- Involved in all stages of the design phase from the initial receipt of the functional product specification through design, simulation and schematic capture down to the layout and final database verification checks.
- Experienced in full custom CMOS layout and design using Cadence Edge and DFII tools operating on Sun Sparc stations, also using Hspice, Silos and Sage simulators integrated within the design framework.
- Used hardware description languages SID (Sagantec) and Verilog-XL for design synthesis and behavioural simulation.

Sept 1983 –June 1990, Plessey Semiconductors, Oldham, England

CAD Process Development Engineer

- Layout and design verification of VLSI bipolar arrays, semi-custom chips and processing-trial chips.
- Responsible for design rule checks, layout vs. schematic checks and pattern generation of completed job using Cadence Dracula software.
- Experienced in use of Caeco design software, Applicon graphics system and Sun microsystems along with Vax-VMS and Unix operating systems.

Training courses

- Magma Vortex (November 2007)
- Cadence Nanoroute (March 2003)
- Verplex Tuxedo LEC (August 2001)
- Avant! Milkyway Cell Library preparation & Apollo Fundamentals (Nov 2000),
- Cadence Advanced SEDSM (Nov 99),
- Cadence SEDSM 5.0 (Apr 98),
- Cadence SKILL for 4.4 (Feb 98),
- Sagantec Dream and Encore (Sept. 96 & Jan 00).

Education

- Sept 1980– June 1983 UCNW Bangor, North Wales
  Mathematics and Electronics BSc (Hons) Joint degree.

Languages

- English, Dutch (2nd language)